IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended): A semiconductor device comprising:

a module substrate having a first main surface and a second main surface facing with the first main surface;

a plurality of substrate-cite interconnects disposed on the first main surface;

a semiconductor chip having top and bottom surfaces, being mounted with a flip chip configuration, configured such that the top surface of [the] said semiconductor chip facing to the first main surface of said module substrate so as to be aligned with said substrate-cite interconnects;

a plurality of joints connected to said substrate-cite interconnects, respectively;

a circuit board having a top surface larger than areas of the first and second main surfaces of said module substrate so that said module substrate is mounted on a localized portion of the top surface and a bottom [surfaces] surface facing with the top surface;

a plurality of board-cite interconnects disposed on the top surface of the circuit board, each being connected to one of said joints in the localized portion of top surface and extending from the localized portion to an outer area on the top surface; and

a first heat conductive material thermally connecting the bottom surface of said semiconductor chip with the top surface of said circuit board.

2. (Original): The semiconductor device of claim 1, further comprising a heat conductive plate in contact with said first heat conductive material.

3.(Original): .The semiconductor device of claim 2, further comprising a second heat conductive material in contact with said heat conductive plate and connecting thermally said heat conductive plate with the bottom surface of said semiconductor chip.

4. (Currently Amended): The semiconductor device of claim 1, further comprising an active element region disposed at the top surface of said semiconductor chip and a plurality of bonding pads surrounding the active element region, the bonding pads disposed at [the] a peripheral region on the top surface of said semiconductor chip.

5. (Original): The semiconductor device of claim 4, further comprising a plurality of bumps, each of bumps is sandwiched between one of said bonding pads and one of the said substrate-cite interconnects.

6. (Original): The semiconductor device of claim 5, further comprising a sealing resin inserted between the top surface of said semiconductor chip and said first main surface of said module substrate.

7. (Currently Amended): The semiconductor device of claim 6, wherein said sealing resin is selectively disposed on [the] a peripheral region of said semiconductor chip so as not to contact with the active element region.

8. (Original): The semiconductor device of claim 7, further comprising a coat-prevention film selectively contacted with the first main surface, disposed just above the active element region.

9. (Original): The semiconductor device of claim 7, further comprising a resin-blocking groove, selectively dug at the first main surface, disposed just above the active element region.

10. (Currently Amended): The semiconductor device of claim 1, further comprising a [chip-shaped] circuit component shaped into a chip configuration adapted for surface mounted technology disposed on the first main surface.

11. (Original): The semiconductor device of claim 1, further comprising a plurality of back interconnects disposed on the second main surface.

12. (Original): The semiconductor device of claim 11, further comprising a plurality of via metals, each connecting one of said back interconnects to one of corresponding substrate-cite interconnects.

13. (Currently Amended): The semiconductor device of claim 12, further comprising a [chip-shaped] circuit component shaped into a chip configuration adapted for surface mounted technology disposed on the second main surface, being configured to connect with one of said back interconnects.

14. (Currently Amended): The semiconductor device of claim 1, further comprising a dielectric spacer disposed on the first main surface, the dielectric spacer having

substantially same thickness as [that] a thickness of said semiconductor chip, enclosing said semiconductor chip and at least partly said joint.

15. (Original): The semiconductor device of claim 14, wherein said substrate-cite interconnects are sandwiched between said dielectric spacer and the first main surface.

16. (withdrawn) A method of assembling a semiconductor device, comprising:

preparing a module substrate having the first main surface and the second main surface facing to said first main surface, a plurality of substrate-cite interconnects being formed on said first main surface;

forming bumps on each of end portions of said substrate-cite interconnects;

mounting a semiconductor chip by a flip chip configuration, facing a top surface thereof to said first main surface, configured such that bonding pads disposed on the top surface of the semiconductor chip contact respectively with said bumps;

forming a plurality of joints on other end portions of said substrate-cite interconnects, respectively; and

mounting said module substrate on a circuit board, configured such that said joints connect to corresponding board-cite interconnects disposed on a top surface of the circuit board, and thermally connecting a bottom surface of said semiconductor chip with the top surface of said circuit board.

17. (Withdrawn) The method of claim 16, further comprising inserting a sealing resin selectively between the peripheral region of said semiconductor chip and the first main

surface, configured such that the sealing resin does not contact with an active element region on the top surface of said semiconductor chip.

18. (Withdrawn) The method of claim 17, further comprising delineating a coat-prevention film on the first main surface before said mounting.

19. (Withdrawn) The method of claim 16, further comprising forming a dielectric spacer on the first main surface, the dielectric spacer having a chip window designed for disposing said semiconductor chip and a plurality of joint windows designed for disposing said joints, configured such that at each bottoms of the joint windows one of said end portions of said substrate-cite interconnects is exposed.

20. (Withdrawn) The method of claim 19, wherein said mounting mounts said semiconductor chip in the chip window, and said forming automatically aligns and positions a plurality of ball electrodes serving as said joints in respective joint windows.